

Sarabjeet Singh

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I am a third year PhD student at the University of Utah, working on efficient memory integrity verification and accelerator for Post Quantum Cryptography, particularly ML as a service with Homomorphic Encryption.

Professional Experience

- **University of Utah** **Salt Lake City, USA**
Research Assistant. Advisor: Prof. Rajeev Balasubramonian
August'20 - Present
- **AMD Research** **Salt Lake City, USA**
Co-op. Project: Processing In Memory
May'20 - August'20
- **University of Utah** **Salt Lake City, USA**
Graduate Assistant
August'19 - May'20
- **Ashoka University, Sonipat** **Sonipat, India**
Junior Research Fellow
September'18 - June'19
- **Indian Institute of Technology, Gandhinagar** **Gandhinagar, India**
Junior Research Fellow
January'18 - August'18
- **Hexagon Capability Center India Hyderabad** **Hyderabad, India**
Software Analyst, Hexagon PPM
August'17 - December'17

Publications

- **CANDLES: Channel-Aware Novel Dataflow-Microarchitecture Co-Design for Low Energy Sparse Neural Network Acceleration**
Sumanth Gudaparthi, Sarabjeet Singh, Surya Narayanan, Rajeev Balasubramonian, Visvesh Sathe
To appear at IEEE International Symposium on High-Performance Computer Architecture (HPCA 2022)
Novel channel-aware dataflow-microarchitecture co-design for sparse networks.
- **Efficacy of Statistical Sampling on Contemporary Workloads: The Case of SPEC CPU2017**
Sarabjeet Singh, Manu Awasthi
2019 IEEE International Symposium on Workload Characterization (IISWC), Orlando, FL, 2019
This work gauges the efficiency of using statistical sampling for simulation of SPEC CPU2017 suite. Our analysis concludes that carefully chosen simulation points faithfully represent the workload: we observe <1% variance in the instruction distribution, while reducing simulation time by $\sim 750\times$.
- **Memory Centric Characterization and Analysis of SPEC CPU2017 Suite**
Sarabjeet Singh, Manu Awasthi
ACM/SPEC International Conference on Performance Engineering (ICPE) 2019, pp. 285-292.
We provide a comprehensive, memory-centric and instruction-level characterization of the SPEC CPU2017 benchmark suite, using a number of mechanisms including dynamic instrumentation, hardware performance counters and OS based tools.
- **PANE: Pluggable Asynchronous Network-on-Chip Simulator**
Sneha N Ved, Sarabjeet Singh, Joyce Meki
ACM Journal on Emerging Technologies in Computing Systems (JETC) 15, no. 1 (2019): 7
In this paper, we propose PANE: Pluggable Asynchronous NETwork-on-Chip simulator, that allows system level simulation and hence, design space exploration of synchronous, asynchronous and heterogeneous NoC for various system level NoC parameters.

Current/Past Research Projects

- **Efficient Integrity Verification using Custom DIMM**
Sarabjeet S., Shreyas S., Rajeev B., Siddharth C. (NVIDIA), Frank M. (Intel) Jan'21 - **Present**
- **Packing and Dataflow for Homomorphic Encryption based Machine Learning accelerator**
Sarabjeet S., Xiong F. (Algorand), Shreyas S., Sumanth G., Rajeev B., Elaine S. (CMU) Aug'21 - **Present**
- **Loss-less FHE-based CNNs - performing non-linear layers on encrypted data**
Sarabjeet Singh, Shreyas Singh, Rajeev Balasubramonian Dec'21 - **Present**
- **Hardware-Software Co-design for accelerating Post Quantum Cryptography**
Sarabjeet S., Xiong F. (Algorand), Ananth K., Lia J., Anirban N., Mahdi B., Rajeev B., Elaine S. (CMU)
- **Secure AI using Samsung's AxDIMM (Finalists for Samsung AxDIMM contest)**
Sarabjeet S., Ananth K., Shreyas S., Lin J., Rajeev B. Oct'21 - **Present**
- **Efficient Metadata for Memory Protection**
Sarabjeet Singh, Meysam Taassori, Rajeev Balasubramonian, Siddharth Chhabra (Intel) Aug'20 - Mar'21
Leveraging locality in memory integrity verification metadata to efficiently cache them on chip.
- **HyGain: high performance, energy-efficient hybrid gain cell based cache hierarchy (arxiv-ed)**
Sarabjeet Singh, Neelam Surana, Pranjali Jain, Joyce Mekie, Manu Awasthi Jan'19 - Nov'19
Investigating the use of novel gain cell design for cache hierarchy, addressing the scalability and power issues of regular SRAM caches.
- **AMBOP: Adaptive Multiple Best Offset Prefetcher**
Archit Checker, Arup Mondal, Sarabjeet Singh, Manu Awasthi Mar'19 - Aug'19
Design of multi-offset prefetcher which learns and issues prefetches taking into consideration the interleaving of memory access patterns.

Education

- **University of Utah** Salt Lake City, USA
PhD in Computer Science, 2019 - Present
- **Indian Institute of Technology, Gandhinagar** Gandhinagar, India
B.Tech. Minor in Computer Science and Engineering, 2013 - 2017
B.Tech. Major in Mechanical Engineering

Awards/Service/Outreach

- One of the finalist for **Samsung's Open Innovation Contest for AxDIMM Technology**.
- **Computer Architecture Student Association (CASA)** Founding Member, Steering Committee (2020-Present)
- **GradSAC, University of Utah** Member (2020-2021)
- **CS 6810 Computer Architecture** Teaching Mentor (Fall 2020)

Blogs/Academic Projects

- **Post Quantum Cryptography**, ACM SigArch Computer Architecture Today Blog
- **Characterizing impact of NoC communication on CNN accelerators**, Advanced Computer Architecture (Spring 2020)
- **Exploring Federated Learning**, Neuromorphic Architectures (Fall 2019)

Technical and Personal skills

- **Programming Languages:** High-level programming languages (C, C++, Python), Assembly language (MIPS), Shell scripting, SQL
- **Familiar Tools:** System Simulators (Sniper, ZSim, Gem5, NVMain, DRAMSim2, USIMM), Interconnection Network Simulators (booksim2, PANE), Performance Analysis Tools and Instrumentation Tools
- **Interests:** Outdoor recreational activities, Snowboarding, Boxing, Men's Mental Health, Animal Welfare

Graduate Coursework

Neuromorphic Architectures, Advanced Computer Architecture, Parallel and High Performance Computing, Digital VLSI Design, Computer Architecture, Distributed Systems, Operating System, Advanced Algorithms

References

- Up to 3 references available on request